UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,245	03/11/2004	Yoshito Date	60188-780	2990

7590 12/12/2006

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
MURALIDAR, RICHARD V	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,245	DATE ET AL.	
	Examiner	Art Unit	
	Richard V. Muralidar	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒- Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/30/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The applicant is advised that the current application is in condition for allowance pending the filing of the terminal disclaimer/s to overcome two double patenting issues; and a certified translation of the applicant's foreign priority document JAPAN 2003-133342, to overcome the 35 U.S.C. 102(e) rejection in view of Date [U.S. 6924601].

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Double Patenting of current application No. 10/797245, based on copending Application No. 11/124265

Claims 1-2, 5-6, 11, 24, 26, 28, 29, and 30 of current Application No. 10/797245 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 12, 13, 16, 17, 20, 21, 23, and 26 of copending Application No. 11/124265. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1-2 are met by claims 13, except claim 13 calls for a transistor, while claims 1-2 recite a specific type of transistor - a MISFET. A MISFET is a type of MOSFET. Furthermore, MOSFETs are well known for their use in display drivers, as exemplified by Cheng [U.S. 2003/0117421], so it would have been obvious to use one to drive a display since applicant claims a display driver. The benefits include fast response time and easy circuit board implementation of the MOSFET. Additionally, these types of display drivers are commonly (if not always) implemented on a chip. For claim 5, claim 17 claims the current mirror and transistors as recited. Claim 6 is met by claim 17. Claim 11 is met by claim 16. Claim 24 is met by claim 12. Claim 26 is met by claims 12 and 20. Claim 28 is met by claim 26. Claim 29 is met by claims 23 and 26. Claim 30 is met by claims 23 and 26.

Application No. 10797245 (the current application) claims:

1. A current driving device provided on a semiconductor chip, comprising: a first-conductive-type first MISFET to which from a reference current source for making a reference current flow, the reference current is transmitted; a first-conductive-type current distribution MISFET which constitutes a current mirror circuit together with the first MISFET and makes the reference current flow; a second-conductive-type current input MISFET connected to the current distribution MISFET; a plurality of current supply sections each including second-conductive-type current source MISFETs constituting a current mirror circuit together with the current input MISFET and an output terminal for outputting a current in accordance with display data; a second-conductive-type current transmission MISFET constituting a current mirror circuit together with the current source MISFETs and the current input MISFET; and a reference current output terminal which is provided on a region of the semiconductor chip located at a distance of 200 .mu.m or less from the current transmission MISFET and outputs a current transmitted from the current transmission MISFET.

2. The current driving device of claim 1, wherein the reference current output terminal is provided on a region of the semiconductor chip located at a distance of 100 .mu.m or less from the current transmission MISFET.

5. The current driving device of claim 1, wherein a current mirror circuit including a first-conductive-type MISFET is further provided on a transmission path through which the reference current is transmitted from the current transmission MISFET to the reference current output terminal.

6. The current driving device of claim 5, wherein a current mirror circuit including a second-conductive-type MISFET is further provided on a transmission path through which the reference current is transmitted from the reference current source to the first MISFET.

11. The current driving device of claim 8, wherein respective gate electrodes of the current distribution MISFETs are connected to a bias line so as to share the bias line with one another, and wherein a resistance element is further provided on

the bias line and between gate respective electrodes of adjacent ones of the current distribution MISFETs.

24. A current driving device comprising: a first-conductive-type first current input MISFET in which a first reference current flows in a driving state; a first-conductive-type second current input MISFET in which a second reference current flows in a driving state; and a plurality of current supply sections each including first-conductive-type current source MISFETs constituting a current mirror circuit together with the first current input MISFET, switches which are connected to the current source MISFETs and turn ON or OFF a current flowing in the current source MISFETs in accordance with display data, a first-conductive-type cascode MISFET which is provided between the current source MISFETs and one of the switches and constitutes a current mirror circuit together with the second current input MISFET, and an output terminal which is connected to the switches and outputs a current in accordance with the display data, the current driving device being provided on a semiconductor chip.

26. A current driving device provided on a semiconductor chip, the device comprising: a first reference current input terminal for receiving a first reference current; a first-conductive-type first current input MISFET to which a current flowing in the first reference current input terminal is transmitted in a first period; a plurality of current supply sections each including first-conductive-type current source MISFETs constituting a current mirror circuit together with the first current input MISFET in the first period and an output terminal for outputting a current in accordance with display data; a first-conductive-type first current transmission MISFET constituting a current mirror circuit together with the first current input MISFET and the current source MISFETs in the first period; a first reference current output terminal to which a current flowing in the first current transmission MISFET is transmitted in the first period; a second reference current input terminal for receiving a second reference current; a first-conductive-type second current input MISFET to which a current flowing in the second reference current input terminal is transmitted in a second period and which constitutes a current mirror circuit together with the current source MISFETs; a first-conductive-type second current transmission MISFET constituting a current mirror circuit together with the current source MISFETs in the second period; a second reference current output terminal to

which a current flowing in the second current transmission MISFET is transmitted in the second period; a first switch provided on a current transmission path between the first reference current input terminal and the first current input MISFET; a second switch provided on a current transmission path between the first current transmission MISFET and the first reference current output terminal; a third switch provided on a current transmission path between the second reference current input terminal and the second current input MISFET; and a fourth switch provided on a current transmission path between the second current transmission MISFET and the second reference current output terminal.

28. A display device comprising: a display panel in which a pixel circuit including a light emitting element having a luminance variable in accordance with the amount of a supplied current is provided; and a current driving device which is provided on each of a plurality of semiconductor chips arranged in a row and supplies a driving current to the pixel circuit, wherein each of the plurality of the semiconductor chips includes a reference current input terminal for receiving a reference current in an end portion and a reference current output terminal for outputting a reference current for a semiconductor chip in a subsequent stage in another end portion, and wherein the reference current input terminal and the reference current output terminal located in adjacent ones of the plurality of the semiconductor chips, respectively, are provided so as to face each other.

29. A display panel comprising: a display panel in which a pixel circuit including a light emitting element having a luminance variable in accordance with the amount of a supplied current is provided; and a plurality of semiconductor chips each including a current driving device for supplying a driving current to the pixel circuit, wherein the current driving device includes a first-conductive-type first MISFET in which a reference current flows in a driving state, a plurality of first-conductive-type current distribution MISFETs which constitutes a current mirror circuit together with the first MISFET and makes the reference current flow, a plurality of second-conductive-type current input MISFETs each having a drain connected to each of the plurality of the current distribution MISFETs, and a plurality of current supply sections each including second-conductive-type current source MISFETs

constituting a current mirror circuit together with the current input MISFET and an output terminal for outputting to the pixel circuit a driving current in accordance with the display data.

30. A display device comprising: a display panel in which a pixel circuit including a light emitting element having a luminance variable in accordance with the amount of a supplied current is provided; and a plurality of semiconductor chips each including a current driving device for supplying a driving current to the pixel circuit, wherein the current driving device includes a first-conductive-type first current input MISFET in which a first reference current flows in a driving state, a first-conductive-type second current input MISFET in which a second reference current flows in a driving state, and a plurality of current supply sections each including first-conductive-type current source MISFETs constituting a current mirror circuit together with the first current input MISFET, switches which are connected to the current source MISFETs and turn ON or OFF a current flowing in the current source MISFETs in accordance with display data, a first-conductive-type cascode MISFET which is provided between the current source MISFETs and the switches and constitutes a current mirror circuit together with the second current input MISFET, and an output terminal which is connected to the switches and outputs to the pixel circuit a driving current in accordance with the display data.

Application No. 11/124265 (the first copending application) claims:

12. A display driver for driving a pixel comprising: a first transistor of a first conductive type; a first reference transistor of the first conductive type constituting a current mirror with the first transistor; a second reference transistor of the first conductive type constituting a current mirror with the first transistor and placed in the vicinity of the first reference transistor; a first current transistor of a second conductive type electrically connected to the first reference transistor and receiving a reference current from the first reference transistor or supplying a reference current to the first reference transistor; a second current transistor of the second conductive type electrically connected to the second reference transistor and receiving a reference current from the

second reference transistor or supplying a reference current to the second reference transistor; a plurality of mirroring transistors of the second conductive type, gate electrodes of the plurality of mirroring transistors electrically connected to each other and electrically connected to both a gate electrode of the first current transistor and a gate electrode of the second current transistor; and a current output circuit electrically connected to the plurality of mirroring transistors and capable of driving a wire connected to the pixel in response to an input digital data.

13. The display driver of claim 12, wherein a distance between the first reference transistor and the second reference transistor is less than or equal to 100.mu.m.

16. The display driver of claim 12, further comprising: a plurality of resistor elements each placed between the gate electrodes of the plurality of mirroring transistors and between a gate electrode of one of the plurality of mirroring transistors and the gate electrode of the first current transistor and between a gate electrode of another one of the plurality of mirroring transistors and the gate electrode of the second current transistor.

17. The display driver of claim 12, further comprising: a third reference transistor of the first conductive type constituting a current mirror with the first transistor and placed in the vicinity of the second reference transistor; and a terminal electrically connected to the third reference transistor and transmitting a reference current from the third reference transistor to outside or from outside to the third reference transistor.

20. The display driver of claim 12, further comprising: a second transistor of the second conductive type electrically connected to the first transistor and receiving a reference current from the first transistor or supplying a reference current to the first transistor; a third transistor of the second conductive type constituting a current mirror with the second transistor; and a terminal electrically connected to the third transistor and transmitting a reference current from the third transistor to outside or from outside to the third transistor.

21. The display driver of claim 20, further comprising: a fourth transistor of the second conductive type electrically connected to the second transistor and receiving a reference current from the second transistor or supplying a reference current to the second transistor; and a fifth transistor of the second conductive type constituting a current mirror with the fourth transistor and receiving a reference current from the third transistor or supplying a reference current to the third transistor.

23. A display driver for driving a pixel comprising: a first transistor of a first conductive type; a second transistor of a second conductive type electrically connected to the first transistor and receiving a reference current from the first transistor or supplying a reference current to the first transistor; a third transistor of the second conductive type constituting a current mirror with the second transistor; a first reference transistor of the first conductive type constituting a current mirror with the first transistor; a second reference transistor of the first conductive type constituting a current mirror with the first transistor and placed in the vicinity of the first reference transistor; a third reference transistor of the first conductive type constituting a current mirror with the first transistor and placed in the vicinity of the second reference transistor; a first current transistor of a second conductive type electrically connected to the first reference transistor and receiving a reference current from the first reference transistor or supplying a reference current to the first reference transistor; a second current transistor of the second conductive type electrically connected to the second reference transistor and receiving a reference current from the second reference transistor or supplying a reference current to the second reference transistor; a plurality of mirroring transistors of the second conductive type, gate electrodes of the plurality of mirroring transistors electrically connected to each other and electrically connected to both a gate electrode of the first current transistor and a gate electrode of the second current transistor; a current output circuit electrically connected to the plurality of mirroring transistors and capable of driving a wire connected to the pixel in response to an input digital data; a first terminal electrically connected to the third reference transistor and transmitting a reference current from the third reference transistor to outside or from outside to the third reference transistor; a second terminal

electrically connected to the third transistor and transmitting a reference current from the third transistor to outside or from outside to the third transistor; and a third terminal electrically connected an intermediate node between the first transistor and the second transistor.

26. A display driving system for driving pixels comprising: a first display driver including: a first transistor of a first conductive type; a first reference transistor of the first conductive type constituting a current mirror with the first transistor; a second reference transistor of the first conductive type constituting a current mirror with the first transistor and placed in the vicinity of the first reference transistor; a first current transistor of a second conductive type electrically connected to the first reference transistor and receiving a reference current from the first reference transistor or supplying a reference current to the first reference transistor; a third reference transistor of the first conductive type constituting a current mirror with the first transistor and placed in the vicinity of the second reference transistor; a first terminal electrically connected to the third reference transistor and transmitting a reference current from the third reference transistor to outside or from outside to the third reference transistor; a first current transistor of a second conductive type electrically connected to the first reference transistor and receiving a reference current from the first reference transistor or supplying a reference current to the first reference transistor; a second current transistor of the second conductive type electrically connected to the second reference transistor and receiving a reference current from the second reference transistor or supplying a reference current to the second reference transistor; a plurality of mirroring transistors of the second conductive type, gate electrodes of the plurality of mirroring transistors electrically connected to each other and electrically connected to both a gate electrode of the first current transistor and a gate electrode of the second current transistor; and a current output circuit electrically connected to the plurality of mirroring transistors and capable of driving a wire connected to a pixel in response to an input digital data; a second display driver including: a first transistor of the first conductive type; a second transistor of the second conductive type electrically connected to the first transistor and receiving a reference current from the first transistor or supplying a reference current to the first transistor; a third transistor of the second conductive

type constituting a current mirror with the second transistor; a second terminal electrically connected to the third transistor and transmitting a reference current from the third transistor to outside or from outside to the third transistor a first reference transistor of the first conductive type constituting a current mirror with the first transistor; a second reference transistor of the first conductive type constituting a current mirror with the first transistor and placed in the vicinity of the first reference transistor; a first current transistor of the second conductive type electrically connected to the first reference transistor and receiving a reference current from the first reference transistor or supplying a reference current to the first reference transistor; a second current transistor of the second conductive type electrically connected to the second reference transistor and receiving a reference current from the second reference transistor or supplying a reference current to the second reference transistor; a plurality of mirroring transistors of the second conductive type, gate electrodes of the plurality of mirroring transistors electrically connected to each other and electrically connected to both a gate electrode of the first current transistor and a gate electrode of the second current transistor; and a current output circuit electrically connected to the plurality of mirroring transistors and capable of driving a wire connected to a pixel in response to an input digital data; and an electric wire electrically connected the first terminal of the first display driver to the second terminal of the second display driver.

This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Double Patenting of current application No. 10/797245, based on copending Application No. 10/815800

Claims 1, 5, 6, 7, 8, 11-16, and 22-30 of current Application No. 10/797245 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 2, 4, 15-17, 19, and 21-22 of copending Application No. 10/815800. Although the conflicting claims are not identical, they are not patentably distinct from each other because they both require a display driver implemented on a chip, comprising first and second conductive transistors (the MISFET being a type of), current references and current supply sections, which are the same thing, and the output terminal located 100/200 micrometers from the current transmission. The examiner also notes that MOSFETs are a commonly used transistor to implement driver display circuits onto a chip, and that MOSFETs and MISFETs are essentially the same, insofar that a MISFET is a type of MOSFET. Also, a pixel is not required, since it is for "driving a pixel." Claim 1 is met by claims 1 and 2. Claim 5 is met by claim 1. Claim 6 is met by claims 1 and 21. Claim 7 is met by claims 2 and 22. For claim 8, all transistors are on the same chip in claim 1. Claim 11 is met by the combination of claims 1 and 17. Claim 12 is met by claim 1. Claim 13 is met by claim 1. Claim 14 is met by claim 19. Claim 15 is met by claim 5. Claim 16 is met by claim 1. Claim 22 is met by claim 17. Claim 23 is met by claim 1. Claim 24 is met by claims 1 and 19. Claim 25 is met by claim 4. Claim 26 is met by claims 1 and 19. Claim 27 is met by claim 1. Claim 28 is met by claim 1. Claim 29 is met by claims 1 and 19. Claim 30 is met by claims 1 and 19.

Application No. 10/815800 (the second copending application) claims:

1. A current driver integrated on a semiconductor chip, comprising: a first current distribution MISFET of a first conductivity type, a source of the first current distribution MISFET being supplied with a supply voltage; a first current input MISFET of a second conductivity type, a drain of the first current input MISFET being connected to a drain of the first current distribution MISFET, the drain and a gate electrode of the first current input MISFET being connected to each other; a second current input MISFET of a second conductivity type, the second current input MISFET and the first current input MISFET constituting a current mirror circuit, a drain and a gate electrode of the second current input MISFET being connected to each other; a first bias line for connecting the gate electrode of the first current input MISFET and the gate electrode of the second current input MISFET; a plurality of current supply sections each including a current source MISFET, the current source MISFET, the first current input MISFET and the second current input MISFET constituting a current mirror circuit, a gate electrode of the current source MISFET being connected to the first bias line; a second current distribution MISFET of the first conductivity type, the second current distribution MISFET and the first current distribution MISFET constituting a current mirror circuit, a drain of the second current distribution MISFET being connected to the drain of the second current input MISFET; a third current distribution MISFET provided adjacent to the second current distribution MISFET, the third current distribution MTSFET, the first current distribution MISFET and the second current distribution MISFET constituting a current mirror circuit; and a first current output terminal which is connected to a drain of the third current distribution MISFET.

2. The current driver of claim 1, wherein the distance between the second current distribution MISFET and the third current distribution MISFET is equal to or shorter than 200 mu.m.

4. The current driver of claim 1, further comprising: at least one additional current distribution MISFET of the first conductivity type provided in a region of the semiconductor chip which is distant from the third current distribution MISFET by 200 .mu.m or less, the additional current distribution MISFET, the second current distribution MISFET and the third current

distribution MISFET constituting a current mirror; and an additional current output terminal which is connected to each of the at least one additional current distribution MISFET.

15. The current driver of claim 14, wherein: the first current distribution MISFET and the second current distribution MISFET constitute a current mirror circuit; and the current-voltage converter is connected to the gate electrode and source of the first current distribution MISFET.

16. The current driver of claim 14, further comprising: a load circuit provided in a region of the semiconductor chip which is distant from the current-voltage converter by 200.mu.m or less; and a current output terminal which is connected to the load circuit.

17. The current driver of claim 14, wherein the load circuit is a first conductivity type MISFET whose drain and gate electrode are connected to each other or a resistor.

21. The display device of claim 19, wherein: the first current driver further includes a bias power supplying terminal which is connected to the gate electrode of the second current distribution MISFET and the gate electrode of the third current distribution MISFET; and the second current driver further includes a fourth current input MISFET of the second conductivity type, a drain and gate electrode of the fourth current input MISFET being connected to each other, the fourth current input MISFET and the third current input MISFET constituting a current mirror circuit between which the plurality of second current supply sections are provided, a bias power input terminal which is connected to the bias power supplying terminal, and a fourth current distribution MISFET of the first conductivity type, a gate electrode of the fourth current distribution MISFET being connected to the bias power input terminal, a drain of the fourth current distribution MISFET being connected to a drain of the fourth current input MISFET.

22. The display device of claim 19, wherein: the first current driver includes at least one additional current distribution MISFET of the first conductivity type provided in a region of the first semiconductor chip which is distant from the third current distribution MISFET by 200.mu.m or less, the additional current distribution MISFET, the second current distribution

MISFET and the third current distribution MISFET constituting a current mirror, and an additional current output terminal which is connected to each of the at least one additional current distribution MISFET; and the second current driver includes a fifth current input MISFET of the second conductivity type, a drain and gate electrode of the fifth current input MISFET being connected for each other, the fifth current input MISFET and the third current input MISFET constituting a current mirror circuit between which the plurality of second current supply sections are provided, and a second current input terminal which is connected to the drain of the fifth current input MISFET and the additional current output terminal.

This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claims 1-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Date [U.S. 6924601].

The applied reference has a common inventor and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claims 1, 12, 24, 26, and 28-30, Date discloses a current driving device [col. 2 lines 49-50] provided on a semiconductor chip [col. 3 lines 34-35], comprising: a first-conductive-type first MISFET to which from a reference current

source for making a reference current flow [col. 3 lines 16-17], the reference current is transmitted; a first-conductive-type current distribution MISFET which constitutes a current mirror circuit together with the first MISFET and makes the reference current flow [col. 3 lines 17-22]; a second-conductive-type current input MISFET connected to the current distribution MISFET; a plurality of current supply sections each including second-conductive-type current source MISFETs [col. 3 lines 17-18] constituting a current mirror circuit together with the current input MISFET and an output terminal for outputting a current in accordance with display data [Fig. 5 terminal 26a]; a second-conductive-type current transmission MISFET constituting a current mirror circuit [col. 3 lines 48-50] together with the current source MISFETs and the current input MISFET; and a reference current output terminal which is provided on a region of the semiconductor chip located at a distance of 200 micrometers [col. 4 lines 3-12] or less from the current transmission MISFET and outputs a current transmitted from the current transmission MISFET [see col. 6-9 first embodiment. The examiner notes that MOSFETs and MISFETs are essentially the same, insofar that a MISFET is a type of MOSFET]. The dependent claims are also substantially disclosed by Date, as shown throughout the disclosure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard V. Muralidar whose telephone number is 571-272-8933. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl D. Easthom can be reached on 571-272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RVM
11/30/2006

KARL EASTHOM
SUPERVISORY PATENT EXAMINER